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(54) **Circuitry implementing the Viterbi algorithm.**

(57) The invention concerns a circuitry implementing the Viterbi algorithm at such a trellis at which each state may be reached along two alternative paths. The states of the bits of a defined time interval are processed utilizing the inventive circuitry in serial form for indicating the symbol including one bit and/or several bits. The invention may be applied, for instance, in the GSM mobile telephone, in which, by the aid of the invention, the signal processing circuits may be saved significantly.

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Circuitry implementing the Viterbi algorithm

The present invention concerns a circuitry arrangement implementing the Viterbi algorithm according to the introduction of claim 1.

The Viterbi algorithm is an algorithm which is commonly used in discharging convolution codes. The Viterbi algorithm is used in receivers of digital transmission systems, for instance in general European digital mobile telephone system (GSM, Groupe Special Mobile), in which digital data to be transmitted to a radio path is on one hand encoded specifically (convolutional coding), and on the other hand, in a transmission chain (transmitter, radio channel, receiver) such mutual effect is produced, which can be processed as unintentional analogous convolutional coding. A coded data signal on the receiving side must be so indicated that the most probable transmitted bit sequence is found therein. The Viterbi algorithm may be used both for said decoding of this code and for indicating the bits of the receiver, in which the unintentional analogous convolutional code produced by the mutual effect of the transmission chain is decoded, and for decoding the channel coding (convolutional coding).

Fig. 1 presents the Viterbi-Trellis encoding known in itself in the art, which forms the basis for the present invention, and its functioning. Each received bit (BIT_k, BIT_{k+1}) includes 16 potential STATES. Each state is associated with a cumulative value CUM describing how probable, or 'good', a path is from the beginning of a bit pattern, that is, from the beginning of a given time interval, to said state. Fig. 1 also presents (within the scope of the trellis presented in this connection) the permitted transitions from one state to another. Each transition is associated with a transition value TRANS determining the 'goodness' of each transition. Each state may, in the present trellis, be en tered along two alternative paths. When the cumulative values CUM_k of the starting state of the previous bit BIT_k and the transition values $TRANS_k$ are added, a 'goodness value' CUM_{k+1} is obtained for each potential state of the next bit BIT_{k+1}, from which the 'goodness' of the bit path from the beginning of the time interval may be derived. Since 16 states may be provided and two paths may lead to each state, there may be 32 transition values j.

Fig. 2 demonstrates the states associated with each bit DET.BIT: the previous state OLD STATE and the new state NEW STATE, to which the above mentioned CUM values are related and the bit-specific potential transitions wherebetween the TRANS values illustrate.

By comparing the 'goodness' of the two paths entering into each state, the better one of these may be selected. The sum of the cumulative value CUM_k of the initial state of the selected path and of the transition value $TRANS_k$ is stored to be the cumulative value of the next state, that is, of a newer bit BIT_{k+1}. For each bit, 16 states i must be calculated, the cumulative values $CUM_k(i)$ of the states thereof being stored in a trace back table (Trace Back, TB).

The conventionally above described Viterbi algorithm is implemented by circuits positioned in parallel (e.g. one circuit per each bit space, 16 parallel circuits in the present case). The great number of circuits raises the equipment cost. In addition, the great number of components for instance in the GSM mobile telephone increases the current consumption.

The object of the invention is to eliminate or to reduce the above adverse factors.

The aim is solved by utilizing the circuitry presented in the characteristic features part of claim 1.

By processing serially the data associated with each possible state of the bit being examined, or in sequence, the circuitry can be made very simple. The processing of the above described Viterbi algorithm regarding each state is carried out. 16 states are calculated in sequence for each bit, the values associated therewith being stored in a trace back table. When all bits of said time interval have been processed, the tracing of a return path is done on the basis of the stored values, whereby the potentially best path is followed from the end to the beginning. In this manner, each bit and/or the symbols related to the bits of the time interval is/are indicated.

The same circuitry may be used e.g. in the GSM mobile telephone to indicate the bit sequence of the receiver, and in addition, discharging of channel-specific decoding (channel decoding) may be accomplished. An advantage of the simple implementation is reduced current consumption, which e.g. in the battery operated GSM telephone is a remarkable advantage. The circuitry of the invention may be implemented as an integrated circuit, such as the VLSI circuit.

According to the principles of the invention, it is also feasible to implement any other Viterbi algorithm, in which a trellis such as the one presented in Fig. 1 is employed.

The invention is described below by the aid of the figures of a drawing, in which

Fig. 1 presents the operation of the known Viterbi-Trellis algorithm in table form,

Fig. 2 presents, simplifying, the state-of-art presentation principle of a bit being examined by the aid of the values associated with two states,

Fig. 3 presents the block diagram of the circuitry of the invention implementing the Viterbi algorithm in serial form, and

Fig. 4 presents the principle block diagram of the tracing of the return path.

Fig. 3 presents the circuitry of the invention applicable e.g. in the presentation and/or channel decoding of the bits received in the GSM mobile telephone. As the input data for the circuitry are provided the 32 transition values TRANS(j), TRANS(j + 1) connected to one bit BIT(k + 1), which are shifted into the transition value table TT. The cumulative values CUM(i) of the previous bit are stored in table CT (CUM Table), from which they are carried into adders ADD; into another adder ADD through a delay circuit L (Latch). The addition of the transition values TRANS and cumulative values CUM related to each state is carried out in the adder. The sums thus obtained are compared in a subtraction unit SUB. With the aid of the most significant bit MSB of the subtraction the selector unit SEL selects a higher sum for a new cumulative value NEW, stored in the table of cumulative values CT. The difference DF of the subtraction (Difference), being scaled in a desired number of bits, is stored in the Trace Back Table TB.

All states included in a given bit are calculated in the same way sequentially, or in serial form, and the results are stored in tables CT, TB. After the calculation of one bit has been completed, the transition values associated with the next bit are read, and the same sequence is started again. The calculation is repeated for all bits of a given time interval. ('Time interval' may in the present connection mean e.g. the frame of the GSM system provided with 148 bits).

When all bits of a time interval have been processed, the tracing of the return path is carried out. Fig. 4 shows a principle block diagram of the circuitry implementing this step. The 'best' path, that is, the description of a path, is read in Table TB (Fig. 3). The topmost bit MSB(T) (the most significant bit) of the difference DF stored in Table TB is equivalent to the indicated bit, and it expresses along which path, according to the trellis, the state of the previous bit can be reached. When said topmost bit MSB(T) is summed up with the value of the state shifted to the left, the value LSB of the next state, when going backwards, is obtained, or the four least significant bits. With the LSB value the value of the next state of the return path memory following from the address location (when going backwards) is presented. In Fig. 4 the circuit L is a delay circuit, and the circuit SL1 (Shift Left One) shifts the value at each moment one bit to the left.

This procedure is repeated for each bit of a time interval, until the entire bit sequence of the time interval has been indicated. Thereafter, the processing of the bits of a next time interval is started.

Claims

1. A circuitry implementing the Viterbi algorithm in a trellis in which each state may be entered along two alternative paths, characterized in that the states of the bits of a defined time interval are processed with the circuitry in serial form for indicating the symbol of a bit and/or several bits.

2. A circuitry according to claim 1, characterized in that it comprises circuits, in which
(a) for each bit (BIT_k) the sum of the transition values ($TRANS_k$) of the values of the cumulative values (CUM(i)) of the states at each moment and of the changes between the bits (BIT_k and BIT_{k+1}) are produced in addition circuits (ADD),
(b) two addition values of each state are compared in a subtraction circuit (SUB),
(c) the result of the comparison (DF) is stored in a trace back path table (TB), and
(d) a new cumulative value (NEW) of the processed bit is selected utilizing a selection circuit which is stored in the table of cumulative values (CT),
whereby the operation (items a through d) is repeated regarding each of the 16 potential states of a bit, and
whereby in the circuitry the entire operation sequence presented above is repeated for each bit in order to determine the return path.

3. A circuitry according to claim 2, characterized in that it comprises furthermore
(e) an indication circuit of a return path, in which on the basis of the bit-specific data (MSBT(T)) read in the trace back path table the address (LSB) of an address location is calculated at each bit of the time interval from which the most probable value of the bit or symbol at a moment can be read,
whereby the bits or symbols of a time interval are indicated starting from the last one.

4. A use of the circuitry according to claim 3 for indicating the bits of a signal flow.

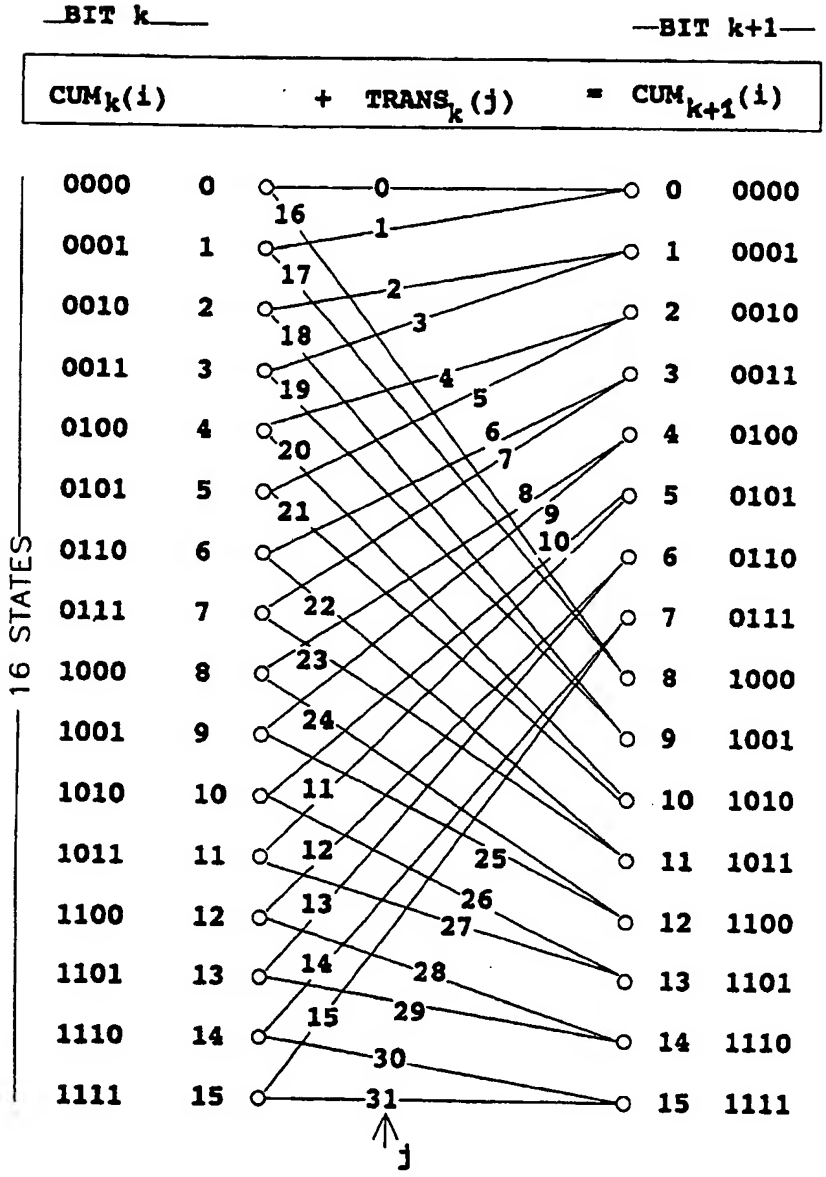
5. A use of the circuitry according to claim 3 for decoding the convolutional code of a signal flow.

6. A use of a circuitry according to claim 3 both for indicating rhe bits of a signal flow and for decoding the convolutional code in the same apparatus.

7. A circuitry according to claim 2 or 3, characterized in that it is implemented as a part of an integrated circuit.

8. A use of a circuitry according to any one of claims 1, 2, 3 or 7 in a mobile telephone of the general European digital mobile telephone system.

VITERBI TRELLIS



TRANS	
0	00000
1	00001
2	00010
3	00011
4	00100
5	00101
6	00110
7	00111
8	01000
9	01001
10	01010
11	01011
12	01100
13	01101
14	01110
15	01111
16	10000
17	10001
18	10010
19	10011
20	10100
21	10101
22	10110
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25	11001
26	11010
27	11011
28	11100
29	11101
30	11110
31	11111

Fig 1

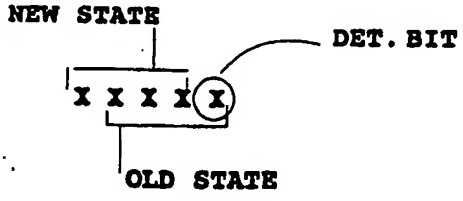

Fig 2

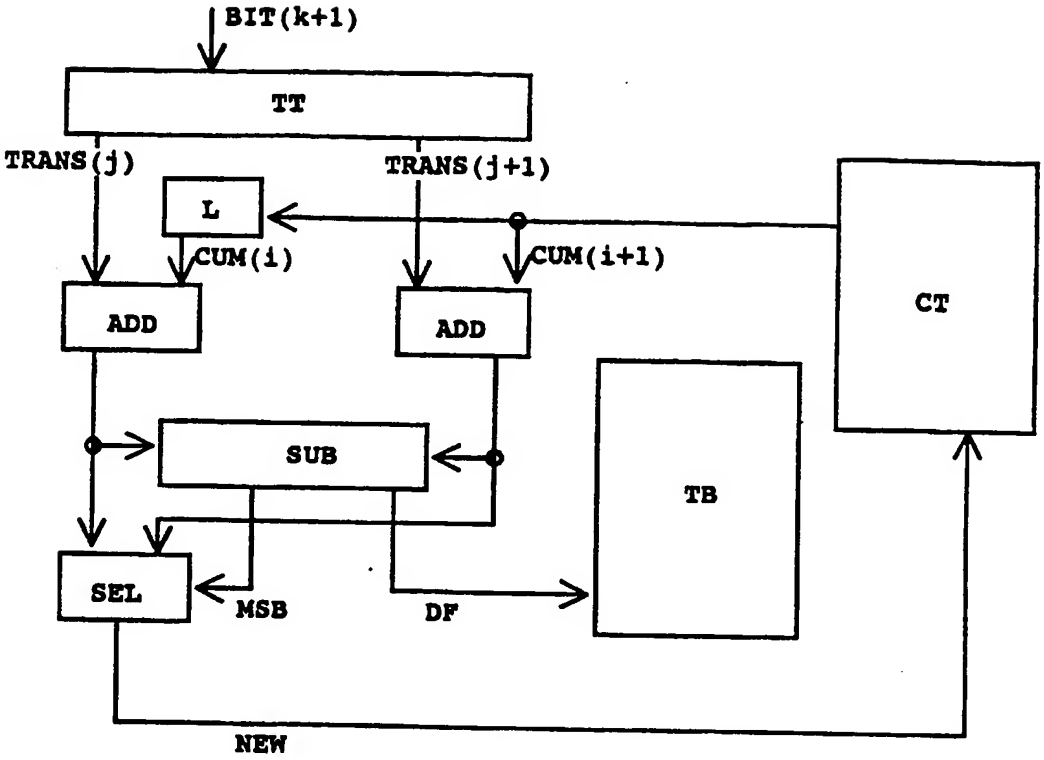
BIT(k+1)
TT
TRANS(j)
TRANS(j+1)
L
CUM(i)
CUM(i+1)
CT
ADD
ADD
SUB
TB
SEL
MSB
DF
NEW

Fig 3

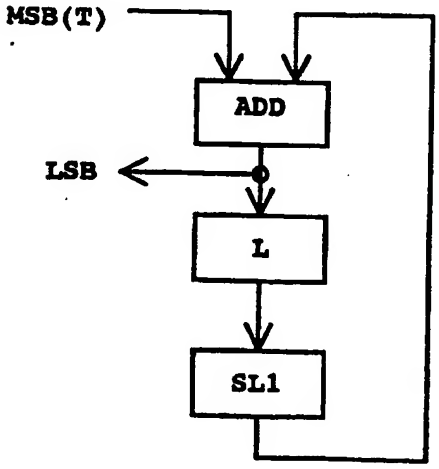
MSB(T)
ADD
LSB
L
SL1

Fig 4